AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A logic circuit optimizing method, comprising:

clustering logic circuits included in inputted logic circuit information to obtain primary clusters;

inserting a flip-flop to a cluster whose cluster length exceeds a predetermined cluster length, the cluster being one of the primary clusters obtained in said clustering; and

re-clustering the flip-flop inserted cluster to obtain secondary clusters,

wherein said inserting a flip-flop to a cluster comprises:

measuring a cluster length of each of the primary clusters obtained in said clustering;

selecting a cluster whose cluster length exceeds the predetermined cluster length, the cluster being one of the primary clusters obtained in said clustering; and

inserting the flip-flop to the selected cluster,

wherein, when there exists a cluster whose cluster length exceeds the predetermined cluster length among the primary clusters obtained in said clustering, said inserting the flip-flop to the selected cluster and said re-clustering the flip-flop inserted cluster are performed.

2. (Canceled)

3. (Currently Amended) The logic circuit optimizing method as defined in claim 1, further comprising:

inserting a flip-flop to a cluster that is too large to be contained in a variable logic element of a logic emulation device, when the cluster is allotted to the variable logic element, the cluster being included in logic circuit information after said clustering and said re-clustering; and

re-clustering the ~~flip-flop inserted~~ cluster that is too large to be contained in the variable logic element of the logic emulation device after the flip-flop has been inserted therein.

4. (Original) The logic circuit optimizing method as defined in claim 1, further comprising: substituting a logic circuit for a to-be-logically-emulated memory device, by expressing a memory device in terms of circuit length, the memory device embodying the to-be-logically-emulated memory device.

5. (Original) The logic circuit optimizing method as defined in claim 4, wherein the circuit length is expressed in terms of a number of cascading circuit stages.

6. (Original) The logic circuit optimizing method as defined in claim 4, wherein the circuit length is expressed in terms of a signal propagation time.

7. (Original) The logic circuit optimizing method as defined in claim 1, wherein the cluster length is expressed in terms of a number of cascading circuit stages.

8. (Original) The logic circuit optimizing method as defined in claim 1, wherein the cluster length is expressed in terms of a signal propagation time.

9. (Currently Amended) A logic circuit optimizing method, comprising:

inserting a flip-flop to a cluster that is too large to be contained in a variable logic element of a logic emulation device, when the cluster is allotted to the variable logic element, the cluster being included in logic circuit information after clustering; and

re-clustering the flip-flop inserted cluster,

wherein an operation clock frequency of the flip-flop which is inserted to the cluster that is too large to be contained in the variable logic element of the logic emulation device is higher than an operation clock frequency of a flip-flop already included in the cluster to which the flip-flop is inserted.

10-11. (Canceled)

12. (Currently Amended) A logic circuit optimizing device, comprising:

a clustering unit operable to cluster logic circuits included in inputted logic circuit information to obtain primary clusters;

a cluster length measuring unit operable to measure a cluster length of each of the primary clusters obtained by said clustering unit;

a selecting unit operable to select a cluster whose cluster length exceeds a predetermined cluster length, the cluster being one of the primary clusters obtained by said clustering unit; and

a circuit dividing unit operable to insert a flip-flop to [[a]] the selected cluster whose cluster length exceeds the predetermined cluster length, the selected cluster being one of the primary clusters obtained by said clustering unit,

wherein said clustering unit is operable to re-cluster ~~re-clusters~~ the flip-flop inserted cluster to obtain secondary clusters.

13. (Canceled)

14. (Currently Amended) The logic circuit optimizing device as defined in claim 12, wherein[[,]] said circuit dividing unit inserts a flip-flop to a cluster that is too large to be contained in a variable logic element of a logic emulation device, when the cluster is allotted to the variable logic element, the cluster being included in logic circuit information after the clustering of the logic circuits by said clustering unit and the re-clustering of the flip-flop inserted cluster; and

wherein said clustering unit re-clusters the ~~flip-flop inserted~~ cluster that is too large to be contained in the variable logic element of the logic emulation device after the flip-flop is inserted therein.

15. (Original) The logic circuit optimizing device as defined in claim 12, further comprising a substitution unit operable to substitute a logic circuit for a to-be-logically-emulated memory device, by expressing a memory device in terms of circuit length, the memory device embodying the to-be-logically-emulated memory device.

16. (Original) The logic circuit optimizing device as defined in claim 15, wherein the circuit length is expressed in terms of a number of cascading circuit stages.

17. (Original) The logic circuit optimizing device as defined in claim 15, wherein the circuit length is expressed in terms of a signal propagation time.

18. (Original) The logic circuit optimizing device as defined in claim 12, wherein the cluster length is expressed in terms of a number of cascading circuit stages.

19. (Original) The logic circuit optimizing device as defined in claim 12, wherein the cluster length is expressed in terms of a signal propagation time.

20. (Currently Amended) A logic circuit optimizing device, comprising:

a circuit dividing unit operable to insert a flip-flop to a cluster that is too large to be contained in a variable logic element of a logic emulation device, when the cluster is allotted to

the variable logic element, the cluster being included in logic circuit information after clustering; and

a clustering unit operable to re-cluster the flip-flop inserted cluster,

wherein an operation clock frequency of the flip-flop which is to be inserted to the cluster that is too large to be contained in the variable logic element of the logic emulation device is higher than an operation clock frequency of a flip-flop already included in the cluster to which the flip-flop is to be inserted.

21-22. (Canceled)